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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,369	06/24/2003	Michael W. Dotson	END920030008US1	1172

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,369	DOTSON ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	17

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment/Remarks and RCE filed on the 02/28/2006 and 05/30/2006. Claims 1-22 are pending.

Response to Arguments

Applicants' arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al. (US Patent No. 6584606 B1) in view of Bassett (US Patent No. 6,242,814).

(Claim 1 and similarly recited claims 8 and 16)

Chiu et al. disclose a system (claim 1)/a computer-implemented method (claim 8)/a program product (claim 16) for positioning I/0 pads (Fig. 1) on a chip, comprising:

an information access system for accessing a control file that includes a proposed placement of a set of I/0 pad groups on the chip (Fig.1; col. 6 lines 6-15; col. 5, ll. 5-15);

a calculation system for calculating (Fig. 1; col.6, lines 51+, see "the solver") a group switching current of a particular I/0 pad group identified in the control file based on individual switching currents of each I/0 pad in the particular I/0 each group (Table

1(" group switching current");col. 6, lines 12-15, lines 40-46; col. 6, ll. 67-col. 7, ll.4; col. 9,ll. 1-30("individual"), lines 40-59("group")), and for comparing the group switching current to a predetermined maximum switching current (Table 1; Fig. 1; col. 6, lines 51+); and

a corrective action system for implementing a corrective action if the group switching current exceeds the predetermined maximum switching current (Fig. 1; col. 7, lines 14-25 ("limit rules"); col.8, lines 1-13).

However, **Chiu et al. do not disclose** the recited limitation "each of the set of I/O pad groups includes at least one power pad" in claims 1, 8, and 16. **Bassett discloses** each of the set of I/O pad groups includes at least one power pad (Figs. 2-3 and 9-10; col. 3, ll. 12-43; col. 4, ll. 45-65; col. 1, ll. 15-30). In addition, **applicants' admitted prior art discloses** the limitation that " each I/O pad group generally includes a power pad for providing the necessary power to the group." (See the application specification, paragraph [0002]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of **Chiu et al.** with the teaching of **Bassett** because the combined teaching would provide a optimized pad structure to accommodate more Vdd and Vss I/O connections without correspondingly increase the die size (Bassett, col. 1, ll. 42- 65).

(Claim 2)

The system of claim 1, wherein the corrective action system (Chiu et al., Fig.1) relocates at least one I/0 pad in the particular I/0 pad group to another I/O pad group if

the group switching current exceeds the predetermined maximum switching current (Chiu et al., col. 7, lines 14+; col. 8, lines 1-23).

(Claim 3)

The system of claim 1, wherein each of the set of I/0 pad groups includes one power pad (Bassett, Figs. 2-3 and 9-10; col. 3, ll. 12-43; col. 4, ll. 45-65; col. 1, ll. 15-30. In addition, **applicants' admitted prior art discloses** the limitation that " each I/O pad group generally includes a power pad for providing the necessary power to the group." (see the application specification, paragraph [0002])).

(Claim 4)

The system of claim 3, wherein the corrective action system inserts an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current (Chiu et al. col.7, line 14 to col. 8 line 26).

(Claim 5)

The system of claim 1, wherein the individual switching currents are determined from an I/O limit table (Chiu et al. col.6, lines 46-50), and wherein the maximum switching current is determined from an information file (Chiu et al. col. 6, lines 51+).

(Claim 6)

The system of claim 1, wherein the chip is a peripheral wire bond chip (Chiu et al. col. 1, line 38-47; col. 5, lines 56-60; col. 7, lines 9-13).

(Claim 7)

The system of claim 1, further comprising an error detection system for detecting and reporting errors in the control file (Chiu et al., Fig. 1; col. 7, lines 14-35).

(Claim 9)

The method of claim 8, wherein the calculating step comprises calculating a group switching current of a particular I/O pad group identified in the control file by summing individual switching currents of each I/O pad in the particular I/O pad group (Chiu et al. ,Table 1; col. 9, lines 40-59).

(Claim 10)

The method of claim 8, wherein the implementing step comprises relocating at least one I/O pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current (Chiu et al. , col. 7, line 14 to col. 8, line 23).

(Claim 11)

The method claim 8, wherein each of the set of I/0 pad groups includes one power pad (Bassett, Figs. 2-3 and 9-10; col. 3, ll. 12-43; col. 4, ll. 45-65; col. 1, ll. 15-30. In addition, **applicants' admitted prior art discloses** the limitation that " each I/O pad group generally includes a power pad for providing the necessary power to the group." (see the application specification, paragraph [0002])).

(Claim 12)

The method of claim 11, wherein the implementing step comprises inserting an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current (Chiu et al., col.7 line 14 to col.8, line 26).

(Claim 13)

The method of claim 8, wherein the individual switching currents are determined from an I/O limit table (Chiu et al., col.6, lines 46-50), and wherein the maximum switching current is determined from an information file (Chiu et al., col. 6, lines 51+).

(Claim 14)

The method of claim 8, further comprising: detecting errors in the control file; and reporting the errors (Chiu et al., Fig. 1; col. 7, lines 14-35).

(Claim 15)

The method of claim 8, wherein the chip is a peripheral wire bond chip (Chiu et al. , col. 1, line 38-47; col. 5, lines 56-60; col. 7, lines 9-13).

(Claim 17)

The program product of claim 16, wherein the program code for implementing a corrective action relocates at least one I/0 pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current (Chiu et al., col. 7, lines 14+; col. 8, lines 1-23).

(Claim 18)

The program product claim 16, wherein each of the set of I/O pad groups includes one power pad (Bassett, Figs. 2-3 and 9-10; col. 3, ll. 12-43; col. 4, ll. 45-65; col. 1, ll. 15-30. In addition, **applicants' admitted prior art discloses** the limitation that " each I/O pad group generally includes a power pad for providing the necessary power to the group." (see the application specification, paragraph [0002])).

(Claim 19)

The program product claim 18, wherein the program code for implementing a corrective action inserts an additional power pad into the particular I/0 pad group if the group switching current exceeds the predetermined maximum switching current (Chiu et al., col.7, line 14 to col. 8 line 26).

(Claim 20)

The program product claim 16, wherein the individual switching currents arc determined from an I/O limit table (Chiu et al., col.6, lines 46-50), and wherein the maximum switching current is determined from an information file (Chiu et al., col. 6, lines 51+).

(Claim 21)

The program product of claim 16, further comprising program code for detecting and reporting errors in the control file (Chiu et al., Fig. 1; col. 7, lines 14-35).

(Claim 22)

The program product of claim l6, wherein the chip is a peripheral wire bond chip (Chiu et al., col. 1, line 38-47; col. 5, lines 56-60; col. 7, lines 9-13).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuyen To

Examiner

AU 2825

PAUL DINH
PRIMARY EXAMINER